INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTY. DOCKET NO. 43876-154	SERIAL NO. Continuation of Serial No. 10/646,787
		APPLICANT Craig HANSEN et al	
(PTO-1449)		FILING DATE Jan. 15, 2004	GROUP To be assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
E.C.		US	5,819,101	10/6/1998	Alexander Peleg, et al	
		US	5,881,275	3/9/1999	Alexander Peleg, et al	
		US	6,119,216	9/12/2000	Alexander Peleg, et al	
		US	6,516,406	2/4/2003	Alexander Peleg, et al	
		US	6,539,467	3/25/2003	Timothy D. Anderson, et al	
		US	6,574,724	6/3/2003	David Hoyle, et al	
E.C.		US	6,631,389 B2	10/7/2003	Derrick Chu Lin, et al	
		US				
		US				
		US				
		US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number --Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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₤ ₵		US 4,785,393	11/15/1988	Chu et al.	
		US 4,814,976	03/21/1989	Craig C. Hansen, et al.	
		US 5,031,135	07/09/1991	Patel	
		US 5,280,598	01/1994	Osaki et al.	
		US 5,481,686	01/02/1996	Dockser	
		US 5,487,024	01/1996	Girardeau Jr.	
		US 5,600,814	02/1997	Gahan et al.	
		US 5,740,093	04/14/1998	Sharangpani	
		US 5,742,840	04/21/1998	Hansen et al.	
		US 5,768,546	06/1998	Kwon	
		US 5,898,849	04/27/1999	Tran	
		US 5,996,057	11/30/1999	Hunter L. Scales, III, et al.	
		US 6,041,404	03/21/2000	Patrice Roussel, etla.	
		US 6,052,769	04/18/2000	Thomas R. Huff, et al	
		US 6,173,393 B1	01/09/2001	Salvador Palanca, et al.	
		US 6,275,834 B1	08/14/2001	Derrick Chu Lin, et al	
₵₰		US 6,295,599	09/2001	Hansen et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code1 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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₤ ₵		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)	
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)	
		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).	
		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).	
₤ ₵		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).	

EXAMINER *Eric Url*	DATE CONSIDERED 4/25/06

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
Є-Ⅼ·	4,025,772	05/24/77	Constant			
	4,489393	12/18/84	Kawahara, et al.			
	4,701,875	10/20/87	Konishi, et al.			
	4,727,505	02/23/88	Konishi, et al.			
	4,876,660	10/24/89	Owens, et al.			
	4,893,267	01/09/90	Alsup, et al.			
	4,956,801	09/11/90	Priem et al.			
	4,969,118	11/06/90	Montoye, et al.			
	4,975,868	12/04/90	Freerksen			
	5,032,865	07/16/91	Schlunt			
	5,157,388	10/20/92	Kohn			
	5,201,056	04/06/93	Daniel, et al.			
	5,268,855	12/07/93	Mason, et al.			
Є.Ⅼ	5,268,995	12/07/93	Diefendorff, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

ЄⅬ·	Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987
Ⅼ.Ⅼ·	Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen; IEEE Micro., April 1992, 40-63
Є.Ⅼ-	Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.
Ⅼ.Ⅼ.	IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, July 31, 1995, 15-16

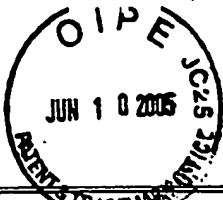| EXAMINER	DATE CONSIDERED
Ɛw ₵ⅼ	4/25/06

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
ℰℓ	5,408,581	04/18/95	Suzuki, et al.			
	5,423,051	06/06/95	Fuller, et al.			
	5,426,600	06/20/95	Nakagawa, et al.			
	5,500,811	03/19/96	Corry			
	5,557,724	09/17/96	Sampat, et al.			
	5,588,152	12/24/96	Dapp, et al.			
	5,592,405	01/07/97	Gove, et al.			
	5,640,543	06/17/97	Farrell, et al.			
	5,642,306	06/24/97	Mennemeier, et al.			
	5,666,298	09/09/97	Peleg, et al.			
	5,669,010	09/16/97	Duluk, Jr.			
	5,673,407	09/30/97	Poland, et al.			
	5,675,526	10/07/97	Peleg, et al.			
ℰℂ	5,680,338	10/21/97	Agarwal, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	No
	0 474 246 A2	06/09/91	Europe				
	0 654 733 A1	05/07/94	Europe				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	The Visual Instruction Set (VIS) in UltraSPARtm, L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, May 3, 1995, 462-469
	Osborne McGraw-Hill, i860tm Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn, 1990, 8-10; 171-175, 182-183
	A General-Purpose Array Processor for Seismic Processing, Nov-Dec., 1984, Volume 1, No. 3) Revisiting past digital signal processor technology, Don Shaver- Jan-Mar. 1998. 5-26
	Accelerating Multimedia with Enhanced Microprocessors, Ruby B. Lee, 1995.

EXAMINER	DATE CONSIDERED 4/25/06

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
(( )	5,721,892	02/24/98	Peleg, et al.	—	—	
	5,734,874	03/31/98	Van Hook, et al.	—	—	
	5,757,432	05/26/98	Dulong, et al.	—	—	
	5,758,176	05/26/98	Agarwal, et al.	—	—	
	5,802,336	09/01/98	Peleg, et al.	—	—	
	5,809,292	09/15/98	Wilkinson, et al.	—	—	
	5,818,739	10/06/98	Peleg, et al.	—	—	
	5,825,677	10/20/98	Agarwal, et al.	—	—	
	5,835,782	11/10/98	Chu Lin, et al.	—	—	
	5,886,732	03/23/99	Humpleman	—	—	
	5,922,066	07/13/99	Cho, et al.	—	—	
	5,983,257	11/09/99	Dulong, et al.	—	—	
	6,016,538	01/18/00	Guttag, et al.	—	—	
	6,092,094	07/18/00	Ireton	—	—	
ƐC	6,401,194 B1	06/04/02	Nguyen, et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

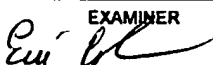|	

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CC·		US	4,658,349 A	05/14/1987	Gafken	
		US	4,852,098	07/25/1989	Brechard et al.	
		US	4,875,161	10/17/1989	Lahti	
		US	4,949,294	08/14/1990	Wambergue	
		US	4,953,073	08/28/1990	Moussouris et al.	
		US	4,959,779	09/25/1990	Weber et al.	
		US	5,113,506	05/12/1992	Moussouris et al.	
		US	5,161,247	11/3/1992	Murakami et al.	
		US	5,208,914	05/04/1993	Wilson et al.	
		US	5,231,646	07/27/1993	Health et al	
		US	5,233,690	08/03/1993	Shelock et al.	
		US	5,268,995	12/07/1993	Diefendorff et al.	
		US	5,347,643 A	09/13/1994	Kondo Nobukazu et al.	
		US	5,412,728 a	05/03/1995	Besnard Christian et al.	
		US	5,430,660 A	07/04/1995	John Hengeveld et al.	
		US	5,471,628	11/28/1995	Phillips et al.	
		US	5,515,520	05/07/1996	Hatta et al.	
		US	5,533,185	07/02/1996	Lentz et al.	
		US	5,590,385	12/31/1996	Ide et al.	
		US	5,636,351	06/03/1997	Lee	
		US	5,742,840	04/21/1998	Hansen et al.	
		US	5,778,412 A	07/07/1998	Gafken	
		US	5,828,869	10/27/1998	Johnson et al.	
		US	5,996,057	11/30/1999	Scales, III et al.	
		US	6,453,388 B2	09/17/2002	Yamamoto	
CR		US	6,657,908 B1	05/20/2003	Furuhashi	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No
CC·		JP 3268024	11/28/1991	Hitachi Ltd.			
		EP 0 468 820 A2	01/29/1992	Fujitsu Limited			
		WO 93/01565	01/21/1993	Seiko Epson Corporation			
		CA 1 323 451	10/19/1993	Northern Telecom Ltd.			
		JP 6095843	04/08/1994	IBM			
		EP 0 651 321 A	05/03/1995	Advanced Micro Devices Inc.			
		EP 0 654 733 A1	05/24/1995	Hewlett-Packard			
		JP-S60-217435	10/31/1985	Toshiba Corp.			
CC,		WO 97/07450	02/27/1997	Microunity Systems Engineering, Inc.			

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£ (·	L-1	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," p. 12-21, 28 March 1993, IEEE J. OF SOLID-STATE CIRCUITS.	
	L-2	K. Uchiyama et al., The Gmicro/500 Superscalar Microprocessor with. Branch Buffers, IEEE Micro, October 1993, p. 12-21.	
	L-3	Ruby B. Lee, Realtime MPEG Video Via Software Decompression on a PA-RISC Processor, IEEE (1995).	
	L-4	Karl M. Guttag et al. "The TMS34010: An Embedded Microprocessor", IEEE June 1988, p. 186-190.	
	L-5	M. Awaga et al., "The µVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation", IEEE Micro, Vol. 13, No. 5, October 1993, p.24-36.	
	L-6	Tom Asprey et al., "Performance Features of the PA7100 Microprocessor", IEEE Micro (June 1993), p. 22-35.	
	L-7	Gove, Robert J., "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conf., March (1994), pp. 215-224.	
	L-8	Woobin Lee, et al., "Mediastation 5000: Integrating Video and Audio," IEEE Multimedia,1994, pp. 50-61.	
	L-9	Karl, Guttag et. al "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, November, 1992, p. 53-64.	
	L-10	TMS320C80 (MVP) Master Processor User's Guide, Texas Instruments, March, 1995, p. 1-33.	
	L-11	TMS320C80 (MVP) Parallel Processor User's Guide ["PP"]; Texas Instruments March 1995, p. 1-80.	
	L-12	Shipnes, Julie, "Graphics Processing with the 88110 RISC Microprocessor," IEEE COMPCOM, (Spring,1992) pp. 169-174.	
	L-13	ILLIAC IV: Systems Characteristics and Programming Manual, May 1, 1972, p. 1-78.	
	L-14	N. Abel et al., ILLIAC IV Doc. No. 233, "Language Specifications for a Fortran-Like Higher Level Language for ILLIAV IV, August 28, 1970, p. 1-51.	
	L-15	ILLIAC IV Quarterly Progress Report: October, November, December 1969; Published January 15, 1970, pp. 1-15.	
𝓔C	L-16	N.E. Abel et al., Extensions to Fortran for Array Processing (1970) pp. 1-16.	

EXAMINER _Eu l/L_   DATE CONSIDERED 4/25/06

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ξ(-	L-17	Morris A, Knapp et al.ILLIAC IV Systems Characteristics and Programming Manual (1972) "Bulk Storage Applications in the ILLIAC IV System," p. 1-10.	
	L-18	Rohrbacher, Donald, et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp 54-59 (August, 1977) (reprinted version pp 119-124).	
	L-19	Siegel, Howard Jay, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6, (June, 1979) (reprinted version pp 110-118).	
	L-20	Mike Chastain, et. al., "The Convex C240 Architecture", Conference of Supercomputing, IEEE 1988, p. 321-329.	
	L-21	Gwennap, Linley, "New PA-RISC Processor Decodes MPEG Video: HP's PA-71 00LC Uses New Instructions to Eliminate Decoder Chip," Microprocessor Report, (January 24, 1994) pp. 16-17.	
	L-22	Patrick Knebel et al., "HP's PA7100LC: A Low-Cost Superscalar PARISC Processor," IEEE (1993), pp. 441-447.	
	L-23	Kurpanek et al., "PA7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," EEEE (1994), pp. 375-82.	
	L-24	Hewlett Packard, PA-RISC 1.1 Architecture and Instruction Set Reference Manual, 3rd ed. Feb. 1994, pp. 1-424.	
	L-25	Margaret Simmons, et. al "A Performance Comparison of Three Supercomputers – Fujitsu VP-2600, NEC SX-3, and Cray Y-MP",. 1991 ACM, p. 150-157.	
	L-26	Smith, J. E., "Dynamic Instruction Scheduling and the Astronautics ZS-1," Computer, Vol. 22, No. 7, July 1989, at 21-35 and/or the Astronautics ZS- 1 computers made used, and/or sold in the United States, pp. 159-173.	
	L-27	Nikhil et al., "T: A Multithreaded Massively Parallel Architecture" Computation Structures Group Memo 325-2 (March 5, 1992) , pp. 1-13.	
ξξ	L-28	Undy, et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE pp. 10-22 (1994).	

EXAMINER	DATE CONSIDERED
(signature)	4/25/06

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EC.	L-29	Feng, Tse-Yun, "Data Manipulating Functions in Parallel Processors and Their Implementations," IEEE Transactions on Computers, Vol. C-23, No. 3, March, 1974 (reprinted version pp. 89-98.	
	L-30	Lawrie, Duncan H., "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. c-24, No. 12, December, 1975 pp. 99-109.	
	L-31	Broomell, George, et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, June, 1983 pp 95-133.	
	L-32	Jain, Vijay, K., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEEICASSP'94 April, 1994 , pp II-521 -- II-524.	
	L-33	Spaderna et al., "An Integrated Floating Point Vector Processor for DSP and Scientific Computing", 1989 IEEE, ICCD, October 1989 p. 8-13.	
	L-34	Gwennap, Linley, "Digital, MIPS Add Multimedia Extensions," Microdesign Resources Nov. 18, 1996 pp. 24-28.	
	L-35	Toyokura, M., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipeline Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.5, 1994 pp. 74-75.	
	L-36	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," Nobuhiro Ide, et. Al. IEEE Tokyo Section, Denshe Tokyo No. 32, 1993, p. 103-109.	
	L-37	Papadopoulos et al., "*T: Integrated Building Blocks for Parallel Computing," ACM (1993) p. 824- and p. 625-63.5	
	L-38	Ruby B. Lee, "Accelerating Multimedia with Enhanced Microprocessors," IEEE Micro April 1995 p. 22-32.	
	L-39	Ruby B. Lee, "Realtime MPEG Video Via Software Decompression on a PA-RISC Processor," IEEE (1995), pp. 186-190.	
	L-40	K. Diefendorff, M. Allen, The Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, p. 157-162.	
EC	L-41	Kristen Davidson, Declaration of Kristen Davidson, p. 1 and H. Takahashi et al., A 289 MFLOPS Single Chip Vector Processing Unit, The Institute of Electronics, Information, and Communication Engineers Technical Research Report, 5/28/92, pp. 17-22.	

EXAMINER	DATE CONSIDERED
Eui EC	4/25/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTY. DOCKET NO. 043876-0154	SERIAL NO. 10/757,515
		APPLICANT HANSEN, C., et al.	
(PTO-1449)		FILING DATE January 15, 2004	GROUP 2183

		OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
*ᶜC	L-42	Kristen Davidson, Declaration of Kristen Davidson, p. 1 and M. Kimura et al., Development of Ginicro 32-bit Family of Microprocessors, Fujitsu Semiconductor Special Part 2, Vol. 43, No. 2, February 1992.	
	L-43	Bit Manipulator," IBM Technical Disclosure Bulletin, November, 1974, pp 1576-1576 https://www.delphion.com/tdbs/tdb?order=75C+0016.	
	L-44	"Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, July, 1986, p. 699-701 https://www.delphion.com/tdbs/tdb?order=86A+61578.	
	L-45	Motorola MC88110 Second Generation RISC Microprocessor User's Manual (1991).	
	L-46	Berkerele, Michael J., "Overview of the START (*T) Multithreaded Computer" IEEE January 1993, p. 148-1 56.	
	L-47	Diefendorff, et al., "Organization of the Motorola 88110 Superscalar RISC Microprocessor" IEEE Micro April, 1992, p.39-63;	
	L-48	Barnes, et al., The ILLIAC IV Computer, IEEE Transactions on Computers, vol. C-17, no. 8, August 1968.	
	L-49	Ruby B. Lee et al., Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7 100LC Processors, Hewlett-Packard J. April 1995, p.60-68.	
	L-50	Ruby B. Lee, "Realtime MPEG Video Via Software Decompression on a PA-RISC Processor," IEEE 1995, p.186-192.	
	L-51	"The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," Robert J. Gove, IEEE DSP Workshop (1994).	
	L-52	Convex Assembly Language Reference Manual, First Ed., December 1991.	
*ᶜCᵢ	L-53	Convex Architecture Reference Manual (C Series), Sixth Edition, Convex Computer Corporation (April 1992).	

EXAMINER	DATE CONSIDERED
ᶜᵤᵢ ᶜₗ	4/25/06

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)		ATTY. DOCKET NO. 043876-0154	SERIAL NO. 10/757,515	
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ƐC	L-54	Manferdelli, et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," submitted to SPIE Annual International Technical Symposium, Sm Diego, Society of Photo Optical Instrumentation Engineers, July 30, 1980, p. 1-8.	
	L-55	Paul Michael Farmwald, Ph.D. "On the Design of High-Performance Digital Arithmetic Units," Thesis, August 1981, p. 1-95.	
	L-56	GsAs Supercomputer Vendors Hit Hard,, Electronic News,1/31/94, 1991, pp. 32.	
	L-57	Convex Adds GaAs System, Electronic News, June 20, 1994.	
	L-58	Kevin Wadleigh et al., High-Performance FFT Algorithms for the Convex C4/XA Supercomputer, Journal of Super Computing, Vol. 9, pp. 163-78 (1995).	
	L-59	Peter Michielse, "Programming the Convex Exemplar Series SPP System, Parallel Scientific Computing, First Intl Workshop, PARA '94, June 20-23, 1994, pp. 375-82.	
	L-60	Ryne, Robert D., "Advanced Computers and Simulation," Los Alamos National Laboratory IEEE 1 993, p. 3229-3233.	
	L-61	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) p. 124-132.	
	L-62	Bell, Gordon, "Ultracomputers: A Teraflop Before its Time," Comm.'s of the ACM Aug. 1992 pp. 27-47.	
	L-63	Geist, G. A., "Cluster Computing: The Wave of the Future?" Oak Ridge National Laboratory, 84OR2 1400 May 30, 1994, p. 236-246.	
	L-64	Vetter et al., "Network Supercomputing," IEEE Network May 1992, p. 38-44.	
	L-65	Renwick, John K." Building a Practical HIPPI LAN," IEEE 1992, p. 355-360.	
	L-66	Tenbrink, et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science 1994 p. 1-4.	
	L-67	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM 1989 p. 1-12.	
	L-68	Watkins, John, et al., "A Memory Controller with an Integrated Graphics Processor," IEEE 1993 p 324-336.	
ƐC	L-69	"Control Data 6400/6500/ 6600 Computer Systems, Instant SMM Maintenance Manual.	

EXAMINER	DATE CONSIDERED
(signature)	4/25/06

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$\mathcal{CC}$	L-70	"Control Data *6400/6500/ 6600* Computer Systems, SCOPE Reference Manual, September1966.	
	L-71	"Control Data *6400/6500/ 6600* Computer Systems, COMPASS Reference Manual, 1969.	
	L-72	Tolmie, Don, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM?" Los Alamos National Laboratory Rep. No. LA-UR 94-3994 (1994).	
	L-73	ILLIAC IV: Systems Characteristics and Programming Manual, May 1, 1972.	
	L-74	1979 Annual Report: The S-1 Project Vol. 1 Architecture 1979.	
	L-75	1979 Annual Report: The S-1 Project Vol.2 Hardware 1979.	
	L-76	S-1 Uniprocessor Architecture, April 21, 1983 (UCID 19782) *See* also S-1 Uniprocessor Architecture (SMA-4), Steven Cornell;	
	L-77	Broughton, et al., The S-1 Project: Top-End Computer Systems for National Security Applications, October 24, 1985.	
	L-78	Convex Data Sheet C4/XA High Performance Programming Environment, Convex Computer Corporation.	
	L-79	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard J. Apr. 1995 p. 79-84.	
	L-80	Mick Bass et al., "The PA 7100LC Microprocessor: A Case Study of Design Decisions in a Competitive Environment Hewlett-Packard J. April 1995, p. 12-18.	
	L-81	Mick Bass, et. al. "Design Methodologies for the PA 7100LC Microprocessor", Hewlett Packard Journal April 1995 p. 23-35.	
	L-82	Wang, Chin-Liang, "Bit-Level Systolic Array for Fast Exponentiation in GF (2Am)," IEEE Transactions on Computers, Vol. 43, No. 7, July, 1994 p. 838-841.	
	L-83	Markstein, P.W., "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, Jan. 1990 p. 111-119.	
	L-84	Donovan, Walt, et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, January, 1995 p. 51- 61.	
	L-85	Ware et al., 64 Bit Monolithic Floating Point Processors, IEEE Journal Of Solid-state Circuits, Vol. Sc-17, No. 5, October 1982, pp. 898-907.	
$\mathcal{CC}$	L-86	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability" (1 993) at 475, p. 898-907.	

EXAMINER	DATE CONSIDERED
Eui C.R	4/25/06

INFORMATION DISCLOSURE CITATION IN AN APPLICATION		ATTY. DOCKET NO. 043876-0154	SERIAL NO. 10/757,515
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₵(-	L-87	Hwang & Degroot, "Parallel Processing for Supercomputers & Artificial Intelligence," 1993.	
	L-88	Nienhaus, Harry A., "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, 1989 pp 1103-1105.	
	L-89	Eisig, David, et al., "The Design of a 64-Bit Integer Multiplier/Divider Unit," IEEE 1993 pp 171-178.	
	L-90	Margulis, Neal, "i860 Microprocessor Architecture," Intel Corporation 1990.	
	L-91	Intel Corporation, 3860 XP Microprocessor Data Book" (May 1991).	
	L-92	Hewlett-Packard, "HP 9000 Series 700 Workstations Technical Reference Manual Model 712 (System)" January 1 994.	
	L-93	Ruby Lee, et al., Pathlength Reduction Features in the PA-RISC Architecture Feb. 24-28, 1992 p. 129-135.	
	L-94	Kevin Wadleigh et al., High Performance FFT Algorithms for the Convex C4/XA Supercomputer, Poster, Conference on Supercomputing, Washington, D.C., Nov. 1994.	
	L-95	Fields, Scott, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin- Madison 1993 p. 1-8.	
	L-96	Litzkow et al., "Condor - A Hunter of Idle Workstations," IEEE (1 988) p. 104-111.	
	L-97	Gregory Wilson, The History of the Development of Parallel Computing" http://ei.cs.vt.edu/-history/Parallel.html, p. 1-38.	
	I-98	Marsha Jovanovic and Kimberly Claffy, Computational Science: Advances Through Collaboration" "Network Behavior" San Diego Supercomputer Center 1993 Science Report, p.1-11 [http://www.sdsc.edu/Publications/SR93/network_behavior.html].	
	L-99	National Science Foundation (NSF) [www.itrd.gov/pubs/blue94/section.4.2.html] 1994.	
	L-100	Intel Corporation, "Paragon User's Guide" (Oct. 1993).	
₵C	L-101	Turcotte, Louis H., "A Survey of Software Environments for Exploiting Networked Computing Resources" Engineering Research Center for Computational Field Simulation June 11, 1993, p. 1-150.	

EXAMINER Eui CL	DATE CONSIDERED 4/25/06

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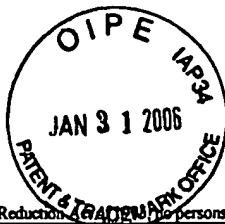
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EC	L-102	Patterson, Barbara, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip" Motorola Computer Group, p. 1-3 [http://badabada.org/misc/mvme197_announce.txt].	
	L-103	Culler, David E., et al., "Analysis Of Multithreaded Microprocessors Under Multiprogramming", Report No. UCBICSD 921687, May 1992 p.1-17.	
	L-104	James Laudon et al., "Architectural And Implementation Tradeoffs In The Design Of Multiple-Context Processors", CSL-TR-92-523, May 1992 p. 1-24.	
	L-105	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," 28 IEEE Custom Integrated Circuits Conference, 1992, p. 30.2.1-30.2.4.	
	L-106	High Speed DRAMs, Special Report, IEEE Spectrum, vol. 29, no. 10, October 1992.	
	L-107	Moyer, Steven A., "Access Ordering Algorithms for a Multicopy Memory," IPC-TR-92-0 1 3, December 18, 1992.	
	L-108	Moyer, Steven A., "Access Ordering and Effective Memory Bandwidth," Ph.D. dissertation, University of Virginia, April 5, 1993.	
	L-109	"Hardware Support for Dynamic Access Ordering: Performance of Some Design Options", Sally McKee, Computer Science Report No. CS-93-08, August 9, 1993.	
	L-110	McGee et al., "Design of a Processor Bus Interface ASIC for the Stream Memory Controller" p. 462-465.	
	L-111	McKee et al., "Experimental Implementation of Dynamic Access Ordering," August 1, 1993, p. 1-10.	
	L-112	McKee et al., Increasing Memory Bandwidth for Vector Computations, Technical Report CS-93-34 August 1, 1993, p.1-18.	
	L-113	Sally A. McKee et al., "Access Order and Memory-Conscious Cache Utilization" Computer Science Report No. CS-94- 10, March 1, 1994, p.1-17.	
EC	L-114	McKee, et. al., "Bounds on Memory Bandwidth in Streamed Computations," Computer Science Report CS-95-32, March 1, 1995.	

EXAMINER	DATE CONSIDERED
[signature]	4/ 25/06

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$\mathcal{E}C$	L-115	McKee, Sally A., "Maximizing Memory Bandwidth for Streamed Computations," A Dissertation Presented to the Faculty of the School of Engineering and Applied Science at the University of Virginia, May 1995.	
	L-116	A Systematic Approach to Optimizing and Verifying Synthesized High-Speed ASICs", Trevor Landon, et. Al. , Computer Science Report No. CS-95-51, December 11, 1995.	
	L-117	"Control Data 6400/6500/ 6600 Computer Systems Reference Manuals" 1969 available at http:/led-thelen.org/comp-hist/CDC-6600-R-M.html ("CDC 6600 Manuals").	
	L-118	"Where now for Media processors?", Nick Flaherty, Electronics Times, August 24, 1998.	
	L-119	George H. Barnes et al., The ILLIAC IV Computer[1] , [1]IEEE Trans., C-17 vol. 8, pp. 746-757, August 1968.	
	L-120	J.E. Thornton, Design of a Computer - The Control Data 6600 (1970) .	
	L-121	Gerry Kane, PA-RISC 2.0 Architecture", Chp. 6 Instruction Set Overview, Prentice Hall isbn 0-13-182734-0, p. 6-1—6-26.	
	L-122	Cosoroaba, A.B., "Synchronous DRAM products revolutionize memory system design," Fujitsu Microelectronics, Southcod95 May 709 1995 .	
	L-123	Intel 450KX/GX PCIset, Inetel Corporation, 1996..	
	L-124	Baland, Granito, Marcotte, Messina, Smith, "The IBM System1360 Model 91 : Storage System" IBM System Journal, January, 1967, pp. 54-68.	
	L-125	File History of U.S. Patent Application No. 08/340,740 (filed November 16, 1994).	
	L-126	File history of U.S. Patent Application No. 07/663,314 (filed March 1, 1991).	
	L-127	S.S. Reddi et. al. "A Conceptual Framework for Computer Architecture" Computing Surveys,. Vol. 8, No. 2, June 1976.	
$\mathcal{E}C$	L-128	Yulun Wang, et al, "The 3DP: A processor Architecture for Three-Dimensional Applications, January 1992, p. 25-36.	

EXAMINER	DATE CONSIDERED
Eui GL	4/25/06

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$\mathcal{C}\mathcal{C}$	L-129	"IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE.	
	L-130	Gerry Kane and Joe Heinrich, "MIPS RISC Architecture" 1992, Publisher: Prentice-Hall Inc., A Simon & Shuster Company, Upper Saddle River New Jersey.	
	L-131	CATHY MAY et al."The Power PC Architecture: A Specification For A New Family of Risc Processors" Second Edition May 1994, pp. 1—518, Morgan Kaufmann Publishers, Inc. San Francisco CA, IBM International Business Machines, Inc.	
	L-132	"IEEE Standard for Scalable Coherent Interface (SCI)" , Published by the Institute of Electrical and Electronics Engineers, Inc. August 2, 2003, pp. 1-248.	
	L-133	DON TOLMIE and Don Flanagan, "HIPPI: It's Not Just for Supercomputers Anymore" Data Communications published May 8, 1995.	
	L-136	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X May 1995.	
	L-137	JOE HEINRICH, "MIPS R4000 Microprocessor User's Manual Second Edition"1994 MIPS Technologies, Inc. pp. 1-754.	
	L-138	Litigation proceedings in the matter of *Microunity Systems Engineering, Inc.* v. *Dell, Inc. et al.*, Corrected Preliminary Invalidity Contentions and Exhibits, filed January 12, 2005, Civil Action No. 2:04-CV-120(TJW), U.S. District Court for the Eastern District of Texas Marshall Division.	
	L-139	Ang, StarT Next Generation: Integrating Global Caches and Dataflow Architecture, Proceedings of the ISCA 1992.	
	L-140	Saturn Architecture Specification, published April 29, 1993.	
	L-141	C4/XA Architecture Overview, Convex Technical Marketing presentation dated November 11, 1993 and February 4, 1994.	
	L-142	Convex 3400 Supercomputer System Overview, published July 24, 1991.	
	L-143	Giloi, Parallel Programming Models and Their Interdependence with Parallel Architectures, IEEE Proceedings published September 1993.	
	L-144	PCT International Search Report and Written Opinion dated March 11, 2005, corresponding to PCT/US04/22126	
$\mathcal{C}\mathcal{C}$	L-145	Supplementary European Search Report dated March 18, 2005, corresponding to Application No. 96928129.4	
EXAMINER			**DATE CONSIDERED** 4/25/06

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				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	1	of	10	Attorney Docket Number	43876-154

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC	AA	US-4,852,098	07/25/1989	Brechard, et al.	
	AB	US-4,875,161	10/17/1989	Lahti, et al.	
	AC	US-4,949,294	08/14/1990	Wambergue, et al.	
	AD	US-4,953,073	08/28/1990	Moussouris, et al.	
	AE	US-4,959,779	09/25/1990	Weber, et al.	
	AF	US-5,081,698	01/14/1992	Kohn	
	AG	US-5,113,506	05/12/1992	Moussouris, et al.	
	AH	US-5,155,816	10/13/1992	Kohn	
	AI	US-5,161,247	11/03/1992	Murakami, et al.	
	AJ	US-5,179,651	01/12/1993	Taaffe, et al.	
	AK	US-5,231,646	07/27/1993	Heath, et al.	
	AL	US-5,233,690	08/03/1993	Sherlock, et al.	
	AM	US-5,241,636	08/31/1993	Kohn	
	AN	US-5,280,598	01/18/1994	Osaki, et al.	
	AO	US-5,487,024	01/23/1996	Girardeau, Jr.	
	AP	US-5,515,520	05/07/1996	Hatta, et al.	
	AQ	US-5,533,185	07/02/1996	Lentz, et al.	
	AR	US-5,590,365	12/31/1996	Ide, et al.	
EC	AS	US-5,600,814	02/04/1997	Gahan, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
EC	AT	WO 93/11500				

Examiner Signature	*Eu. Cl*	Date Considered	4/25/06

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	First Named Inventor	Craig C. HANSEN, et al.
	Group Art Unit	2183
(use as many sheets as necessary)	Examiner Name	CHAN, EDDIE P
Sheet.	2	of	10	Attorney Docket Number	43876-154

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T²
ɕ(	AU	IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)	
ɕ(	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)	
ɕ(	AW	Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 –848)	
ɕ()	AX	IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767)	
ɕ(ı	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228)	
ɕ(	AZ	MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621)	
ɕ(	BA	i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn	
ɕ(	BB	Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900)	· .
ɕ(	BC	Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455)	
ɕ(	BD	Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, pp. 53-64 (November 1992) (51056DOC000913 – 924)	
ɕ(ı	BE	Lee et al., "MediaStation 5000: Integrating Video and Audio," IEEE Multimedia pp. 50-61 (Summer 1994) (51056DOC000901 – 912)	
ɕ(	BF	TMS320C80 (MVP) Parallel Processor User's Guide, Texas Instruments (March 1995) (51056DOC003744 – 4437)	
ɕ(	BG	TMS320C80 (MVP) Master Processor User's Guide, Texas Instruments (March 1995) (51056DOC000925 – 957)	
ɕ(	BH	Bass et al., "The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 12-22 (April 1995) (51056DOC059283 – 289)	
ɕ(	BI	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard Journal, Vol. 46, No. 2, p. 79 (April 1995) (51056DOC059277 – 282)	
ɕ(	BJ	Gwennap, "New PA-RISC Processor Decodes MPEG Video: Hewlett-Packard's PA-7100LC Uses New Instructions to Eliminate Decoder Chip," Microprocessor Report, pp. 16-17 (January 24, 1994) (51056DOC002140 – 141)	
ɕ(	BK	Gwennap, "Digital MIPS Add Multimedia Extensions," Microdesign Resources, pp. 24-28 (November 18, 1996) (51056DOC003454 – 459)	
ɕ(	BL	Kurpanek et al., "PA7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," IEEE COMPCON '94, pp. 375-82 (February 28- March 4, 1994) (51056DOC002149 – 156)	
ɕ(	BM	Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35' (February 24-28, 1992) (51056DOC068161 – 167)	
ɕ(	BN	Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557)	

Examiner Signature	*[signature]*	Dated Considered	4/15/06

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PTO/SB/08a 07-05)
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/757,515
				Filing Date	January 15, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	3	of	10	Attorney Docket Number	43876-154

		U.S. PATENT DOCUMENTS			
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC	BO	US-5,636,351	06/03/1997	Lee	
	BP	US-5,721,892	02/24/1998	Peleg, et al.	
	BQ	US-5,734,874	03/31/1998	Van Hook, et al.	
	BR	US-5,758,176	05/26/1998	Agarwal, et al.	
	BS	US-5,768,546	06/16/1998	Kwon	
	BT	US-5,887,183	03/23/1999	Agarwal, et al.	
	BU	US-5,996,057	11/30/1999	Scales III, et al.	
	BV	US-6,425,073	07/23/2002	Roussel, et al.	
EC	BW	US-6,516,406	02/04/2003	Peleg, et al.	

		FOREIGN PATENT DOCUMENTS				
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Examiner Signature	*[signature]*		Date Considered	4/25/06

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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E.C.	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 – 351)	
	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090)	
	BZ	Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 – 590)	
	CA	HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 – 141)	
	CB	PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 – 176)	
	CC	Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 - 776)	
	CD	Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 – 519)	
	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 – 751)	
	CF	Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 – 763)	
	CG	Nikhil et al., "*T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 – 476)	
	CH	Papadopoulos et al., "*T: Integrated Building Blocks for Parallel Computing," ACM, pp. 624-35 (1993) (51056DOC007278 – 289)	
	CI	Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC069260 – 262)	
	CJ	M. Phillip, "Performance Issues for 88110 RISC Microprocessor," IEEE, 1992 (51056DOC008752 – 757)	
	CK	M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 – 789)	
	CL	R. Mueller, "The MC88110 Instruction Sequencer," Northcon, 1992 (51056DOC009735 – 738)	
	CM	J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 – 742)	
	CN	K. Pepe, "The MC88110's High Performance Load/Store Unit," Northcon, 1992 (51056DOC009743 – 747)	
	CO	J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 – 063)	
	CP	Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 – 646)	
	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661)	
	CR	Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 – 656)	
	CS	Awaga et al., "The µVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
E.C.	CT	Takahashi et al., "A 289 MFLOPS Single Chip Vector Processing Unit," The Institute of Electronics, Information, and Communication Engineers Technical Research Report, pp. 17-22 (May 28, 1992) (51056DOC009798 – 812)	

Examiner Signature	*Eric Cle*	Dated Considered	*4/25/06*

Substitute for form 1449B/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*	Application Number	10/757,515
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	First Named Inventor	Craig C. HANSEN, et al.
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	Examiner Name	CHAN, EDDIE P
Sheet 5 of 10	Attorney Docket Number	43876-154

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
E.C.	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 – 194)	
E.C.	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 – 607)	
E.C.	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)	
E.C.	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034)	
E.C.	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 – 279)	
E.C.	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)	
E.C.	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)	
E.C.	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 – 607)	
E.C.	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 – 918)	
E.C.	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)	
E.C.	DE	Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618)	
E.C.	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)	
E.C.	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)	
E.C.	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)	
E.C.	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)	
E.C.	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)	
E.C.	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)	
E.C.	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)	
E.C.	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)	
E.C.	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 – 7510)	
E.C.	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)	
E.C.	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 – 443)	
E.C.	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 – 459)	
E.C.	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 – 5299)	
E.C.	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)	

Examiner Signature	*Eric U*	Dated Considered	9/25/06

Substitute for form 1449A/PTO				Complete if Known	
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	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 – 666)	
	DW	Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. 1, pp. 275-84 (April 17-20, 1989) (5156DOC070711 – 717)	
	DX	Grimes et al., "The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities," IEEE Computer Graphics & Applications, pp. 85-94 (July 1989) (5156DOC070701 – 710)	
	DY	Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 – 094)	
	DZ	Kohn et al., "A New Microprocessor with Vector Processing Capabilities," Electro/89 Conference Record, pp. 1-6 (April 11-13, 1989) (5156DOC070672 – 678)	
	EA	Kohn et al., "Introducing the Intel i860 64-Bit Microprocessor," IEEE Micro, pp. 15-30 (August 1989) (5156DOC070627 – 642)	
	EB	Kohn et al., "The i860 64-Bit Supercomputing Microprocessor," AMC, pp. 450-56 (1989) (51056DOC000330 – 336)	
	EC	Margulis, "i860 Microprocessor Architecture," Intel Corporation (1990) (51056DOC066610 – 7265 and 5156DOC069971 – 70626)	
	ED	Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 – 700)	
	EE	Patel et al., "Architectural Features of the i860 – Microprocessor RISC Core and On-Chip Caches," IEEE, pp. 385-90 (1989) (5156DOC070679 – 684)	
	EF	Rhodehamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 – 647)	
	EG	Perry, "Intel's Secret is Out," IEEE Spectrum, pp. 22-28 (April 1989) (5156DOC070648 – 654)	
	EH	Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 – 101)	
	EI	i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 – 427)	
	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 – 9097)	
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	
	EP	N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 – 73027)	
	EQ	Hansen, "Architecture of a Broadband Mediaprocessor," IEEE COMPCON 96 (February 25-29, 1996) (MU0013276 – 283 and 51057DOC001825 - 831)	
	ER	Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 – 630)	

Examiner Signature		Dated Considered	4/25/06

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

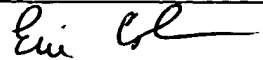| Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
⟨⟨	ES	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958)	
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 – 923)	
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 – 040)	
	EV	Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 – 300)	
	EW	Donovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 – 645)	
	EX	Fields, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin-Madison, http://www.cs.wisc.edu/condor/doc/WiscIdea.html (1993) (51056DOC068704 – 711)	
	EY	Geist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 – 929)	
	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)	
	FA	Giloi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801)	
	FB	Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 – 673)	
	FC	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662)	
	FD	Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 - 1028)	
	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694)	
	FF	Jain et al., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEE ICASSP '94, pp. II-521 – II-524 (April 1994) (51056DOC003070 – 073)	
	FG	Laudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 – 327)	
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 – 942)	
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 - 699)	
	FJ	Litzkow et al., "Condor – A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 – 719)	
	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 – 628)	
	FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 – 471)	
⟨C⟩	FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 – 942)	

Examiner Signature	*Eui Le*	Dated Considered	4/25/06

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EC	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 – 948)	
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 – 887)	
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110 118) (51056DOC002949 – 957)	
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 – 896)	
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)	
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 – 946)	
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 – 609)	
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)	
	FV	Toyokura et al., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipelined Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.5, pp. 74-75 (1994) (51056DOC003659 – 660)	
	FW	Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 – 443)	
	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 – 256)	
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 – 936)	
	FZ	Wang, "Bit-Level Systolic Array for Fast Exponentiation in GF(2m)," IEEE Transactions on Computers, Vol. 43, No. 7, pp. 838-41 (July 1994) (51056DOC059407 – 410)	
	GA	Ware et al., "64 Bit Monolithic Floating Point Processors," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC059646 – 655)	
	GB	"Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206)	
	GC	Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209)	
	GD	Data General AViiON AV500, 550, 4500 and 5500 Servers	
	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)	
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)	
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 – 243)	
EC	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)	

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Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** *(use as many sheets as necessary)*	Complete if Known	
	Application Number	10/757,515
	Filing Date	January 15, 2004
	First Named Inventor	Craig C. HANSEN, et al.
	Group Art Unit	2183
	Examiner Name	CHAN, EDDIE P

Sheet	9	of	10	Attorney Docket Number	43876-154

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T²
EC	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)	
		Original Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	
	GJ	Amended Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	
	GK	Expert Witness Report of Richard A. Killworth, Esq., *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	
	GP	Request for *Inter Partes* Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	. .
	GQ	Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GR	Deposition of Leslie Kohn on September 22, 2005; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GS	Intel Article, *"Intel Announces Record Revenue of 9.96 Billion"*, October 18, 2005	
	GT	The New York Times Article, *"Intel Posts 5% Profit Increase on Demand for Notebook Chips"*, October 19, 2005	
	GU	USA Today Article, *"Intel's Revenue Grew 18% In Robust Quarter for Tech"*, October 19, 2005	
	GV	The Wall Street Journal Article, *"Intel Says Chip Demand May Slow"*, October 19, 2005	
EC	GW	The New York Times Article, *"Intel Settlement Revives A Fading Chip Designer"*, October 20, 2005	

Examiner Signature	*[signature]*	Dated Considered	4/25/06

INFORMATION DISCLOSURE CITATION IN AN APPLICATION	ATTY. DOCKET NO. 043876-0154	SERIAL NO. 10/757,515
	APPLICANT Craig HANSEN, et al.	
(PTO-1449)	FILING DATE January 15, 2004	GROUP 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC.	A	US	6,643,765	11-04-2003	Hansen et al.	
EC	B	US	6,725,356	04-20-2004	Hansen et al.	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
EC	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)	
EC	D	Intel Press Release, "Intel Announces Record Revenue of $9.96 Billion," Santa Clara, CA, 10-18-2005	

EXAMINER Eric Cu	DATE CONSIDERED 4/25/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.